

Features

- Single Voltage Read/Write Operation: 2.65V to 3.3V
- Access Time – 70 ns
- Sector Erase Architecture
 - Thirty-one 32K Word (64K Bytes) Sectors with Individual Write Lockout
 - Eight 4K Word (8K Bytes) Sectors with Individual Write Lockout
- Fast Word Program Time – 20 μ s
- Fast Sector Erase Time – 300 ms
- Low-power Operation
 - 30 mA Active
 - 10 μ A Standby
- Data Polling, Toggle Bit, Ready/Busy for End of Program Detection
- VPP Pin for Write Protection and Accelerated Program/Erase Operations
- $\overline{\text{RESET}}$ Input for Device Initialization
- Sector Lockdown Support
- Minimum 100 Write Cycles

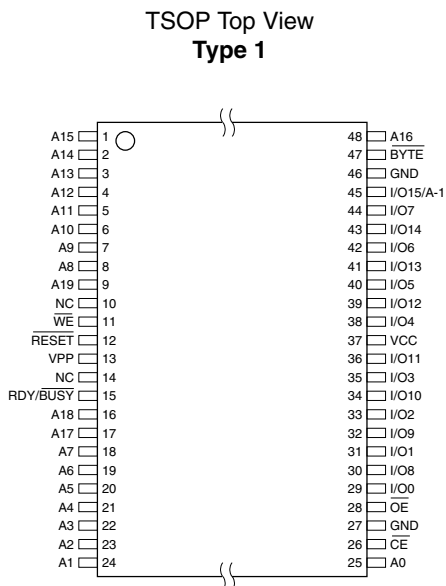
Description

The AT47BV161T is a 3.0-volt 16-megabit Flash memory organized as 1,048,576 words of 16 bits each or 2,097,152 bytes of 8 bits each. The x16 data appears on I/O0 - I/O15; the x8 data appears on I/O0 - I/O7. The memory is divided into 39 sectors for erase operations. The device is offered in a 48-lead TSOP package. The device has $\overline{\text{CE}}$ and $\overline{\text{OE}}$ control signals to avoid any bus contention. This device can be read or reprogrammed using a single 2.65V power supply, making it ideally suited for in-system programming.

The device powers on in the read mode. Command sequences are used to place the device in other operation modes such as program and erase. The device has the capability to protect the data in any sector. (See “Sector Lockdown” section.)

Pin Configurations

Pin Name	Function
A0 - A19	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
$\overline{\text{RESET}}$	Reset
$\text{RDY}/\overline{\text{BUSY}}$	READY/BUSY Output
VPP	Write Protection and Power Supply for Accelerated Program/Erase Operations
I/O0 - I/O14	Data Inputs/Outputs
I/O15 (A-1)	I/O15 (Data Input/Output, Word Mode) A-1 (LSB Address Input for Read Operations in Byte Mode)
BYTE	Selects Byte or Word Mode for Read Operations
NC	No Connect



**16-megabit
(1M x 16/2M x 8)
3-volt Only
Flash Memory**

AT47BV161T



The end of a program or an erase cycle is detected by the Ready/Busy pin, Data Polling or by the toggle bit.

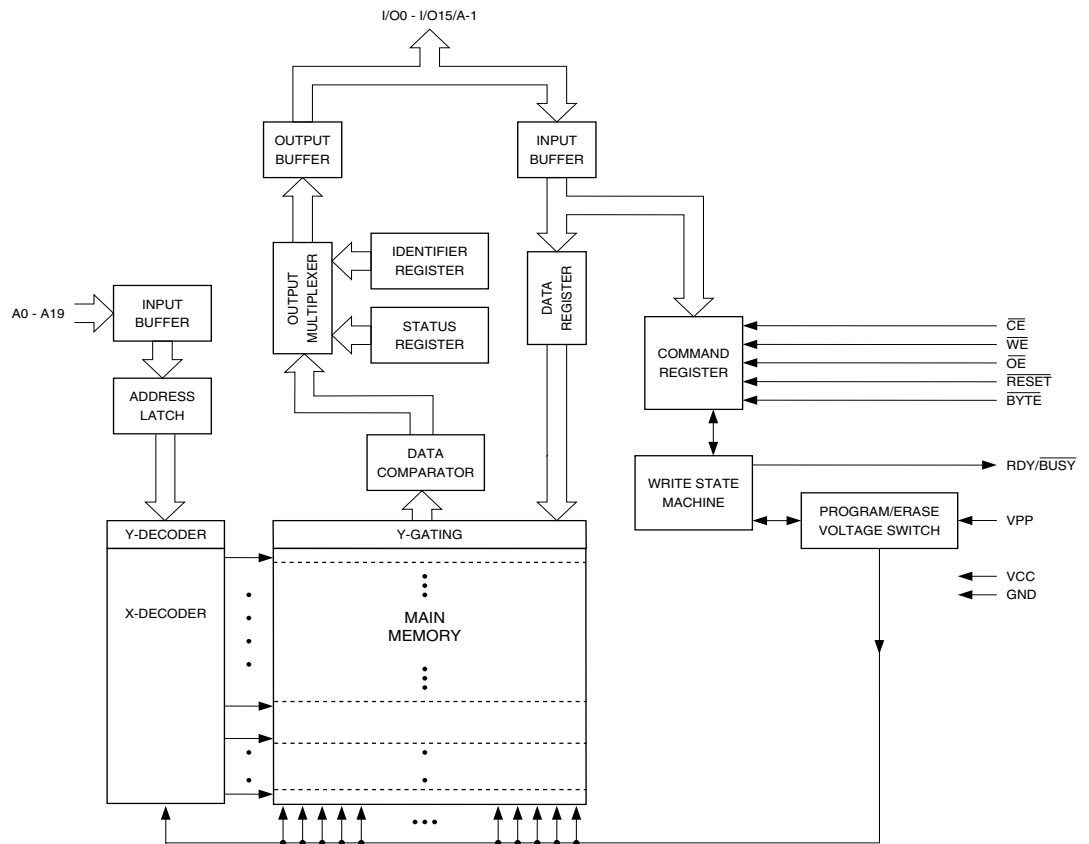
The VPP pin provides data protection and faster programming. When the VPP input is below 0.8V, the program and erase functions are inhibited. When VPP is at 1.65V or above, normal program and erase operations can be performed. With VPP at 5.0V or 12.0V, the program and erase operations are accelerated.

A six-byte command (Enter Single Pulse Program Mode) sequence to remove the requirement of entering the three-byte program sequence is offered to further improve programming time. After entering the six-byte code, only single pulses on the write control lines are required for writing into the device. This mode (Single Pulse Word Program) is exited by powering down the device, or by pulsing the RESET pin low for a minimum of 500 ns and then bringing it back to VCC. The Erase command will not work while in this mode; if entered it will result in data being programmed into the device. It is not recommended that the six-byte code reside in the software of the final product but only exist in external programming code.

During a read operation, the BYTE pin controls whether the device data I/O pins operate in the byte or word configuration. If the BYTE pin is set at logic "1", the device is in word configuration, I/O0 - I/O15 are active and controlled by CE and OE. If the BYTE pin is set at logic "0", the device is in byte configuration, and only data I/O pins I/O0 - I/O7 are active and controlled by CE and OE. The data I/O pins I/O8 - I/O14 are tri-stated, and the I/O15 pin is used as an input for the LSB (A-1) address function.

During a programming operation, the BYTE pin must be set at logic "1", and thus the device always operates in the Word mode.

Block Diagram



Device Operation

READ: The AT47BV161T is accessed like an EPROM. When \overline{CE} and \overline{OE} are low and \overline{WE} is high, the data stored at the memory location determined by the address pins are asserted on the outputs. The outputs are put in the high-impedance state whenever \overline{CE} or \overline{OE} is high. This dual-line control gives designers flexibility in preventing bus contention.

COMMAND SEQUENCES: When the device is first powered on, it will be reset to the read or standby mode, depending upon the state of the control line inputs. In order to perform other device functions, a series of command sequences are entered into the device. The command sequences are shown in the "Command Definition in Hex" table on page 10 (I/O8 - I/O15 are don't care inputs for the command codes). The command sequences are written by applying a low pulse on the \overline{WE} or \overline{CE} input with \overline{CE} or \overline{WE} low (respectively) and \overline{OE} high. The address is latched on the falling edge of \overline{CE} or \overline{WE} , whichever occurs last. The data is latched by the first rising edge of \overline{CE} or \overline{WE} . Standard microprocessor write timings are used. The address locations used in the command sequences are not affected by entering the command sequences.

RESET: A \overline{RESET} input pin is provided to ease some system applications. When \overline{RESET} is at a logic high level, the device is in its standard operating mode. A low level on the \overline{RESET} input halts the present device operation and puts the outputs of the device in a high-impedance state. When a high level is reasserted on the \overline{RESET} pin, the device returns to the read or standby mode, depending upon the state of the control inputs.

ERASURE: Before a word can be reprogrammed, it must be erased. The erased state of memory bits is a logical "1". The entire device can be erased by using the Chip Erase command or individual sectors can be erased by using the Sector Erase command.

CHIP ERASE: The entire device can be erased at one time by using the six-byte chip erase software code. After the chip erase has been initiated, the device will internally time the erase operation so that no external clocks are required. The maximum time to erase the chip is t_{EC} .

If the sector lockdown has been enabled, the chip erase will not erase the data in the sector that has been locked out; it will erase only the unprotected sectors. After the chip erase, the device will return to the read or standby mode.

SECTOR ERASE: As an alternative to a full chip erase, the device is organized into 39 sectors (SA0 - SA38) that can be individually erased. The Sector Erase command is a six-bus cycle operation. The sector address is latched on the falling \overline{WE} edge of the sixth cycle while the 30H data input command is latched on the rising edge of \overline{WE} . The sector erase starts after the rising edge of \overline{WE} of the sixth cycle. The erase operation is internally controlled; it will automatically time to completion. The maximum time to erase a sector is t_{SEC} . When the sector programming lockdown feature is not enabled, the sector will erase (from the same Sector Erase command). An attempt to erase a sector that has been protected will result in the operation terminating in 2 μ s.

WORD PROGRAMMING: Once a memory block is erased, it is programmed (to a logical "0") on a word-by-word basis. Programming is accomplished via the internal device command register and is a four-bus cycle operation. The device will automatically generate the required internal program pulses.



Any commands written to the chip during the embedded programming cycle will be ignored. If a hardware reset happens during programming, the data at the location being programmed will be corrupted. Please note that a data “0” cannot be programmed back to a “1”; only erase operations can convert “0”s to “1”s. Programming is completed after the specified t_{BP} cycle time. The Data Polling feature or the Toggle Bit feature may be used to indicate the end of a program cycle. If the erase/program status bit is a “1”, the device was not able to verify that the erase or program operation was performed successfully.

VPP PIN: The circuitry of the AT47BV161T is designed so that the device can be programmed or erased from the V_{CC} power supply or from the VPP input pin. When V_{PP} is greater than 1.65V and less than or equal to the VCC pin, the device selects the V_{CC} supply for programming and erase operations. When the VPP pin is greater than the V_{CC} supply, the device will select the V_{PP} input as the power supply for programming and erase operations. The device will allow for some variations between the V_{PP} input and the V_{CC} power supply in its selection of V_{CC} or V_{PP} for program or erase operations. If the VPP pin is within 0.3V of V_{CC} for $2.65V < V_{CC} < 3.3V$, then the program or erase operations will use V_{CC} and disregard the V_{PP} input signal. When the V_{PP} signal is used for program and erase operations, the V_{PP} must be in the $5V \pm 0.5V$ or $12V \pm 0.5V$ range to ensure proper operation. The V_{pp} pin cannot be left floating.

PROGRAM/ERASE STATUS: The device provides several bits to determine the status of a program or erase operation: I/O2, I/O3, I/O5, I/O6 and I/O7. The “Status Bit Table” on page 9 and the following four sections describe the function of these bits. To provide greater flexibility for system designers, the AT47BV161T contains a programmable configuration register. The configuration register allows the user to specify the status bit operation. The configuration register can be set to one of two different values, “00” or “01”. If the configuration register is set to “00”, the part will automatically return to the read mode after a successful program or erase operation. If the configuration register is set to a “01”, a Product ID Exit command must be given after a successful program or erase operation before the part will return to the read mode. It is important to note that whether the configuration register is set to a “00” or to a “01”, any unsuccessful program or erase operation requires using the Product ID Exit command to return the device to read mode. The default value (after power-up) for the configuration register is “00”. Using the four-bus cycle Set Configuration Register command as shown in the “Command Definition in Hex” table on page 10, the value of the configuration register can be changed. Voltages applied to the RESET pin will not alter the value of the configuration register. The value of the configuration register will affect the operation of the I/O7 status bit as described below.

DATA POLLING: The AT47BV161T features Data Polling to indicate the end of a program cycle. If the status configuration register is set to a “00”, during a program cycle an attempted read of the last word loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. During a chip or sector erase operation, an attempt to read the device will give a “0” on I/O7. Once the program or erase cycle has completed, true data will be read from the device. Data Polling may begin at any time during the program cycle. Please see “Status Bit Table” on page 9 for more details.

If the status bit configuration register is set to a “01”, the I/O7 status bit will be low while the device is actively programming or erasing data. I/O7 will go high when the device has completed a program or erase operation. Once I/O7 has gone high, status information on the other pins can be checked.

The $\overline{\text{Data}}$ Polling status bit must be used in conjunction with the erase/program and V_{PP} status bit as shown in the algorithm in Figures 1 and 2 on page 7.

TOGGLE BIT: In addition to $\overline{\text{Data}}$ Polling, the AT47BV161T provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the memory will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle. Please see “Status Bit Table” on page 9 for more details.

The toggle bit status bit should be used in conjunction with the erase/program and V_{PP} status bit as shown in the algorithm in Figures 3 and 4 on page 8.

ERASE/PROGRAM STATUS BIT: The device offers a status bit on I/O5, which indicates whether the program or erase operation has exceeded a specified internal pulse count limit. If the status bit is a “1”, the device is unable to verify that an erase or a word program operation has been successfully performed. The device may also output a “1” on I/O5 if the system tries to program a “1” to a location that was previously programmed to a “0”. Only an erase operation can change a “0” back to a “1”. If a program (Sector Erase) command is issued to a protected sector, the protected sector will not be programmed (erased). The device will go to a status read mode and the I/O5 status bit will be set high, indicating the program (erase) operation did not complete as requested. Once the erase/program status bit has been set to a “1”, the system must write the Product ID Exit command to return to the read mode. The erase/program status bit is a “0” while the erase or program operation is still in progress. Please see “Status Bit Table” on page 9 for more details.

V_{PP} STATUS BIT: The AT47BV161T provides a status bit on I/O3, which provides information regarding the voltage level of the VPP pin. During a program or erase operation, if the voltage on the VPP pin is not high enough to perform the desired operation successfully, the I/O3 status bit will be a “1”. Once the V_{PP} status bit has been set to a “1”, the system must write the Product ID Exit command to return to the read mode. On the other hand, if the voltage level is high enough to perform a program or erase operation successfully, the V_{PP} status bit will output a “0”. Please see “Status Bit Table” on page 9 for more details.

SECTOR LOCKDOWN: Each sector has a programming lockdown feature. This feature prevents programming of data in the designated sectors once the feature has been enabled. These sectors can contain secure code that is used to bring up the system. Enabling the lockdown feature will allow the boot code to stay in the device while data in the rest of the device is updated. This feature does not have to be activated; any sector’s usage as a write-protected region is optional to the user.

At power-up or reset, all sectors are unlocked. To activate the lockdown for a specific sector, the six-bus cycle Sector Lockdown command must be issued. Once a sector has been locked down, the contents of the sector is read-only and cannot be erased or programmed.





SECTOR LOCKDOWN DETECTION: A software method is available to determine if programming of a sector is locked down. When the device is in the software product identification mode (see “Software Product Identification Entry/Exit” sections on page 19), a read from address location 00002H within a sector will show if programming the sector is locked down. If the data on I/O0 is low, the sector can be programmed; if the data on I/O0 is high, the program lockdown feature has been enabled and the sector cannot be programmed. The software product identification exit code should be used to return to standard operation.

SECTOR LOCKDOWN OVERRIDE: The only way to unlock a sector that is locked down is through reset or power-up cycles. After power-up or reset, the content of a sector that is locked down can be erased and reprogrammed.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product.

For details, see “Operating Modes” on page 12 (for hardware operation) or “Software Product Identification Entry/Exit” on page 19. The manufacturer and device codes are the same for both modes.

RDY/BUSY: For the AT47BV161T, an open-drain RDY/BUSY output pin provides another method of detecting the end of a program or erase operation. RDY/BUSY is actively pulled low during the internal program and erase cycles and is released at the completion of the cycle. The open-drain connection allows for OR-tying of several devices to the same RDY/BUSY line. Please see “Status Bit Table” on page 9 for more details.

HARDWARE DATA PROTECTION: The Hardware Data Protection feature protects against inadvertent programs to the AT47BV161T in the following ways: (a) V_{CC} sense: if V_{CC} is below 1.8V (typical), the program function is inhibited. (b) V_{CC} power-on delay: once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 10 ms (typical) before programming. (c) Program inhibit: holding any one of OE low, CE high or WE high inhibits program cycles. (d) Noise filter: pulses of less than 15 ns (typical) on the WE or CE inputs will not initiate a program cycle. (e) Program inhibit: V_{PP} is less than V_{ILPP} . (f) V_{PP} power-on delay: once V_{PP} has reached 1.65V, program and erase operations can occur after 100 ns.

INPUT LEVELS: While operating with a 2.65V to 3.3V power supply, the address inputs and control inputs (OE, CE and WE) may be driven from 0 to 5.5V without adversely affecting the operation of the device. The I/O lines can only be driven from 0 to $V_{CC} + 0.6V$.

Figure 1. Data Polling Algorithm
(Configuration Register = 00)

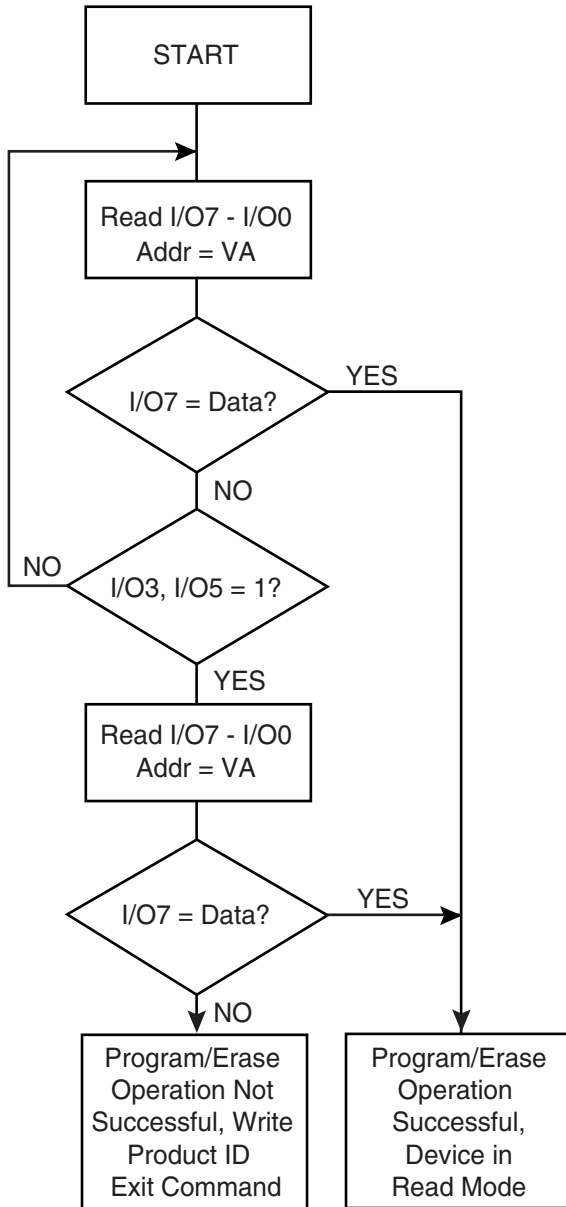
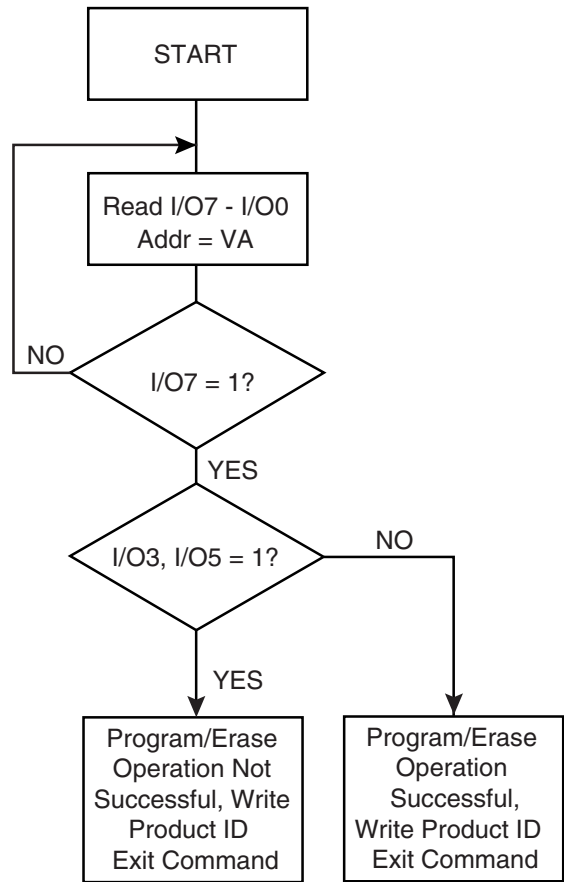


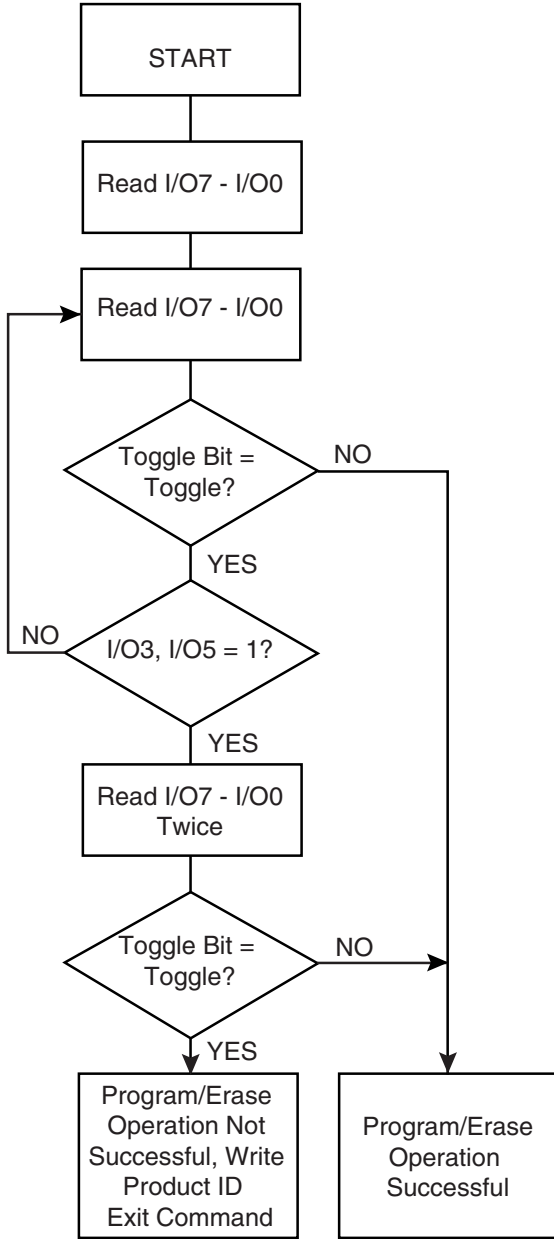
Figure 2. Data Polling Algorithm
(Configuration Register = 01)



Note: 1. VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.

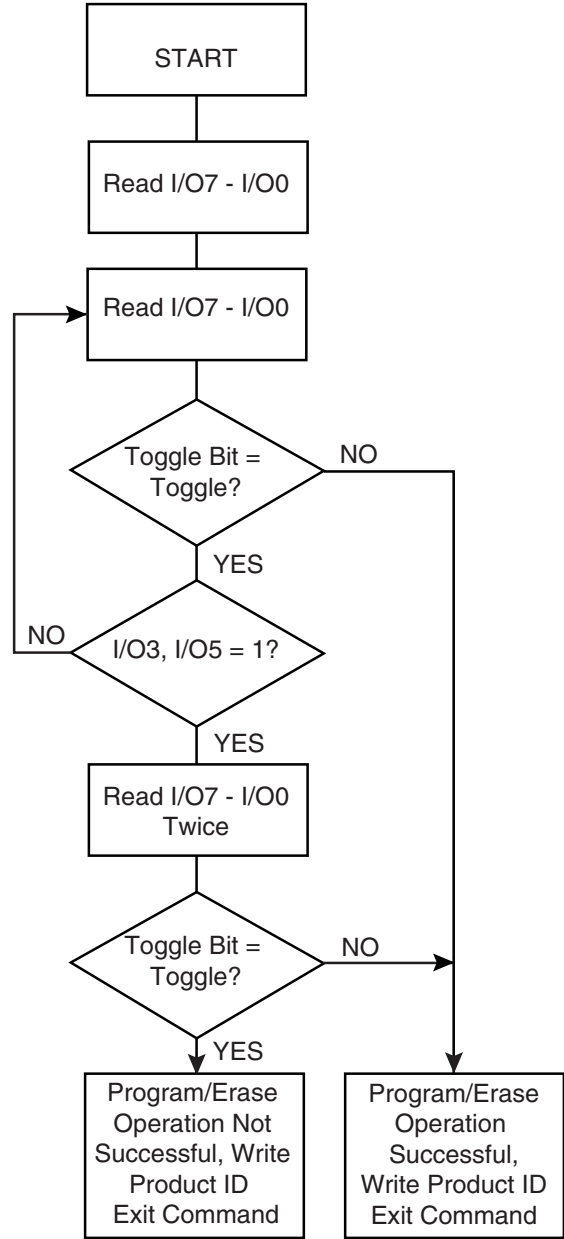
- Notes:
1. VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.
 2. I/O7 should be rechecked even if I/O5 = "1" because I/O7 may change simultaneously with I/O5.

Figure 3. Toggle Bit Algorithm
(Configuration Register = 00)



Note: 1. The system should recheck the toggle bit even if I/O5 = "1" because the toggle bit may stop toggling as I/O5 changes to "1".

Figure 4. Toggle Bit Algorithm
(Configuration Register = 01)



Note: 1. The system should recheck the toggle bit even if I/O5 = "1" because the toggle bit may stop toggling as I/O5 changes to "1".

Status Bit Table

	Status Bit						
	I/O7	I/O7	I/O6	I/O5 ⁽¹⁾	I/O3 ⁽²⁾	I/O2	RDY/ <u>BUSY</u>
Configuration Register:	00	01	00/01	00/01	00/01	00/01	00/01
Programming	<u>I/O7</u>	0	TOGGLE	0	0	1	0
Erasing	0	0	TOGGLE	0	0	TOGGLE	0

- Notes:
1. I/O5 switches to a "1" when a program or an erase operation has exceeded the maximum time limits or when a program or sector erase operation is performed on a protected sector.
 2. I/O3 switches to a "1" when the V_{PP} level is not high enough to successfully perform program and erase operations.



Command Definition in Hex⁽¹⁾

Command Sequence	Bus Cycles	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	1	Addr	D _{OUT}										
Chip Erase	6	555	AA	AAA ⁽²⁾	55	555	80	555	AA	AAA	55	555	10
Sector Erase	6	555	AA	AAA	55	555	80	555	AA	AAA	55	SA ⁽³⁾⁽⁴⁾	30
Word Program	4	555	AA	AAA	55	555	A0	Addr	D _{IN}				
Enter Single Pulse Program Mode	6	555	AA	AAA	55	555	80	555	AA	AAA	55	555	A0
Single Pulse Word Program	1	Addr	D _{IN}										
Sector Lockdown	6	555	AA	AAA	55	555	80	555	AA	AAA	55	SA ⁽³⁾⁽⁴⁾	60
Product ID Entry	3	555	AA	AAA	55	555	90						
Product ID Exit ⁽⁵⁾	3	555	AA	AAA	55	555	F0						
Product ID Exit ⁽⁵⁾	1	XXX	F0										
Set Configuration Register	4	555	AA	AAA	55	555	D0	XXX	00/01 ⁽⁶⁾				

- Notes:
1. The DATA FORMAT shown for each bus cycle is as follows; I/O7 - I/O0 (Hex). In word operation I/O15 - I/O8 are Don't Care. The ADDRESS FORMAT shown for each bus cycle is as follows: A11 - A0 (Hex). Address A19 through A11 are Don't Care in the word mode. Address A19 through A11 and A-1 are Don't Care in the byte mode.
 2. Since A11 is a Don't Care, AAA can be replaced with 2AA.
 3. SA = sector address. Any word address within a sector can be used to designate the sector address (see page 11 for details).
 4. Once a sector is in the lockdown mode, data in the protected sector cannot be changed unless the chip is reset or power cycled.
 5. Either one of the Product ID Exit commands can be used.
 6. The default state (after power-up) of the configuration register is "00".

Absolute Maximum Ratings*

Temperature under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V _{CC} + 0.6V
Voltage on \overline{OE} and V _{PP} with Respect to Ground	-0.6V to +13.0V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AT47BV161T – Sector Address Table

Sector	Size (Bytes/Words)	x8 Address Range (A19 - A-1)	x16 Address Range (A19 - A0)
SA0	64K/32K	000000 - 00FFFF	00000 - 07FFF
SA1	64K/32K	010000 - 01FFFF	08000 - 0FFFF
SA2	64K/32K	020000 - 02FFFF	10000 - 17FFF
SA3	64K/32K	030000 - 03FFFF	18000 - 1FFFF
SA4	64K/32K	040000 - 04FFFF	20000 - 27FFF
SA5	64K/32K	050000 - 05FFFF	28000 - 2FFFF
SA6	64K/32K	060000 - 06FFFF	30000 - 37FFF
SA7	64K/32K	070000 - 07FFFF	38000 - 3FFFF
SA8	64K/32K	080000 - 08FFFF	40000 - 47FFF
SA9	64K/32K	090000 - 09FFFF	48000 - 4FFFF
SA10	64K/32K	0A0000 - 0AFFFF	50000 - 57FFF
SA11	64K/32K	0B0000 - 0BFFFF	58000 - 5FFFF
SA12	64K/32K	0C0000 - 0CFFFF	60000 - 67FFF
SA13	64K/32K	0D0000 - 0DFFFF	68000 - 6FFFF
SA14	64K/32K	0E0000 - 0EFFFF	70000 - 77FFF
SA15	64K/32K	0F0000 - 0FFFFF	78000 - 7FFFF
SA16	64K/32K	100000 - 10FFFF	80000 - 87FFF
SA17	64K/32K	110000 - 11FFFF	88000 - 8FFFF
SA18	64K/32K	120000 - 12FFFF	90000 - 97FFF
SA19	64K/32K	130000 - 13FFFF	98000 - 9FFFF
SA20	64K/32K	140000 - 14FFFF	A0000 - A7FFF
SA21	64K/32K	150000 - 15FFFF	A8000 - AFFFF
SA22	64K/32K	160000 - 16FFFF	B0000 - B7FFF
SA23	64K/32K	170000 - 17FFFF	B8000 - BFFFF
SA24	64K/32K	180000 - 18FFFF	C0000 - C7FFF
SA25	64K/32K	190000 - 19FFFF	C8000 - CFFFF
SA26	64K/32K	1A0000 - 1AFFFF	D0000 - D7FFF
SA27	64K/32K	1B0000 - 1BFFFF	D8000 - DFFFF
SA28	64K/32K	1C0000 - 1CFFFF	E0000 - E7FFF
SA29	64K/32K	1D0000 - 1DFFFF	E8000 - EFFFF
SA30	64K/32K	1E0000 - 1EFFFF	F0000 - F7FFF
SA31	8K/4K	1F0000 - 1F1FFF	F8000 - F8FFF
SA32	8K/4K	1F2000 - 1F3FFF	F9000 - F9FFF
SA33	8K/4K	1F4000 - 1F5FFF	FA000 - FAFFF
SA34	8K/4K	1F6000 - 1F7FFF	FB000 - FBFFF
SA35	8K/4K	1F8000 - 1F9FFF	FC000 - FCFFF
SA36	8K/4K	1FA000 - 1FBFFF	FD000 - FDFFF
SA37	8K/4K	1FC000 - 1FDFFF	FE000 - FEFFF
SA38	8K/4K	1FE000 - 1FFFFF	FF000 - FFFFF





DC and AC Operating Range

		AT47BV161T-70	AT47BV161T-90
Operating Temperature (Case)	Ind.	-40°C - 85°C	-40°C - 85°C
V _{CC} Power Supply		2.65V to 3.3V	2.65V to 3.3V

Operating Modes

Mode	\overline{CE}	\overline{OE}	\overline{WE}	RESET	V _{PP}	Ai	I/O
Read	V _{IL}	V _{IL}	V _{IH}	V _{IH}	X	Ai	D _{OUT}
Program/Erase ⁽²⁾	V _{IL}	V _{IH}	V _{IL}	V _{IH}	V _{IHPP} ⁽⁶⁾	Ai	D _{IN}
Standby/Program Inhibit	V _{IH}	X ⁽¹⁾	X	V _{IH}	X	X	High-Z
Program Inhibit	X	X	V _{IH}	V _{IH}	X		
	X	V _{IL}	X	V _{IH}	X		
	X	X	X	V _{IH}	V _{ILPP} ⁽⁷⁾		
Output Disable	X	V _{IH}	X	V _{IH}	X		High-Z
Reset	X	X	X	V _{IL}	X	X	High-Z
Product Identification							
Hardware	V _{IL}	V _{IL}	V _{IH}	V _{IH}		A1 - A19 = V _{IL} , A9 = V _H ⁽³⁾ , A0 = V _{IL}	Manufacturer Code ⁽⁴⁾
						A1 - A19 = V _{IL} , A9 = V _H ⁽³⁾ , A0 = V _{IH}	Device Code ⁽⁴⁾
Software ⁽⁵⁾				V _{IH}		A0 = V _{IL} , A1 - A19 = V _{IL}	Manufacturer Code ⁽⁴⁾
						A0 = V _{IH} , A1 - A19 = V _{IL}	Device Code ⁽⁴⁾

- Notes:
- X can be V_{IL} or V_{IH}.
 - Refer to AC programming waveforms on page 18.
 - V_H = 12.0V ± 0.5V.
 - Manufacturer Code: 1FH (x8); 001FH (x16), Device Code: C2H (x8); 00C2H (x16).
 - See details under "Software Product Identification Entry/Exit" on page 19.
 - V_{IHPP} (min) = 1.65V; V_{IHPP} (max) = 3.6V. For faster erase/program operations, V_{PP} can be set to 5.0V ± 0.5V or 12V ± 0.5V.
 - V_{ILPP} (max) = 0.8V.

DC Characteristics

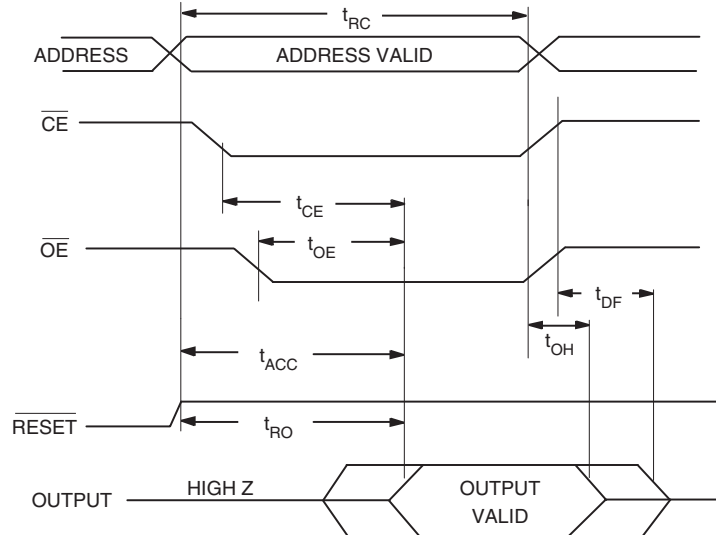
Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	$V_{IN} = 0V$ to V_{CC}		10	μA
I_{LO}	Output Leakage Current	$V_{I/O} = 0V$ to V_{CC}		10	μA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE} = V_{CC} - 0.3V$ to V_{CC}		10	μA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE} = 2.0V$ to V_{CC}		1	mA
I_{SB3}	V_{CC} Standby Current TTL	$\overline{CE} = 2.0V$ to V_{CC} , $V_{CC} = 2.85V$		10	μA
$I_{CC}^{(1)}$	V_{CC} Active Read Current	$f = 5$ MHz; $I_{OUT} = 0$ mA, $3.3V \leq V_{CC}$		30	mA
I_{CC1}	V_{CC} Programming Current ($V_{PP} = V_{CC}$)			45	mA
I_{PP1}	V_{PP} Input Load Current	$V_{PP} = 0V$, $V_{CC} = 3.0V$		10	μA
		$V_{PP} = V_{CC} = 3.0V$		10	μA
I_{CC2}	V_{CC} Programming Current ($V_{PP} = 5.0V \pm 0.5V$)			40	mA
I_{PP2}	V_{PP} Programming Current ($V_{PP} = 5.0V \pm 0.5V$)			5	mA
I_{CC3}	V_{CC} Programming Current ($V_{PP} = 12.0V \pm 0.5V$)			40	mA
I_{PP3}	V_{PP} Programming Current ($V_{PP} = 12.0V \pm 0.5V$)			6	mA
V_{IL}	Input Low Voltage			0.6	V
V_{IH}	Input High Voltage		2.0		V
V_{OL1}	Output Low Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{OL2}	Output Low Voltage	$I_{OL} = 1.0$ mA		0.20	V
V_{OH1}	Output High Voltage	$I_{OH} = -400$ μA	2.4		V
V_{OH2}	Output High Voltage	$I_{OH} = -100$ μA	2.5		V

Note: 1. In the erase mode, I_{CC} is 50 mA.

AC Read Characteristics

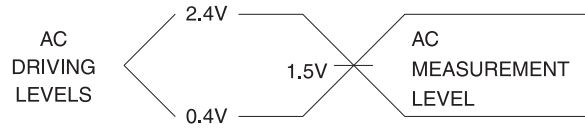
Symbol	Parameter	AT47BV161T-70		AT47BV161T-90		Units
		Min	Max	Min	Max	
t_{RC}	Read Cycle Time		70		90	ns
t_{ACC}	Address to Output Delay		70		90	ns
$t_{CE}^{(1)}$	\overline{CE} to Output Delay		70		90	ns
$t_{OE}^{(2)}$	\overline{OE} to Output Delay	0	35	0	40	ns
$t_{DF}^{(3)(4)}$	\overline{CE} or \overline{OE} to Output Float	0	25	0	25	ns
t_{OH}	Output Hold from \overline{OE} , \overline{CE} or Address, whichever occurred first	0		0		ns
t_{RO}	\overline{RESET} to Output Delay		100		100	ns

AC Read Waveforms⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

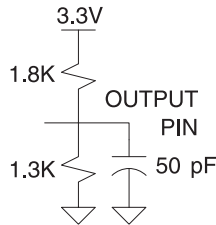


- Notes:
- \overline{CE} may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC} .
 - \overline{OE} may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of \overline{CE} without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC} .
 - t_{DF} is specified from \overline{OE} or \overline{CE} , whichever occurs first (CL = 5 pF).
 - This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



Output Test Load



Pin Capacitance

f = 1 MHz, T = 25°C⁽¹⁾

Symbol	Typ	Max	Units	Conditions
C _{IN}	4	6	pF	V _{IN} = 0V
C _{OUT}	8	12	pF	V _{OUT} = 0V

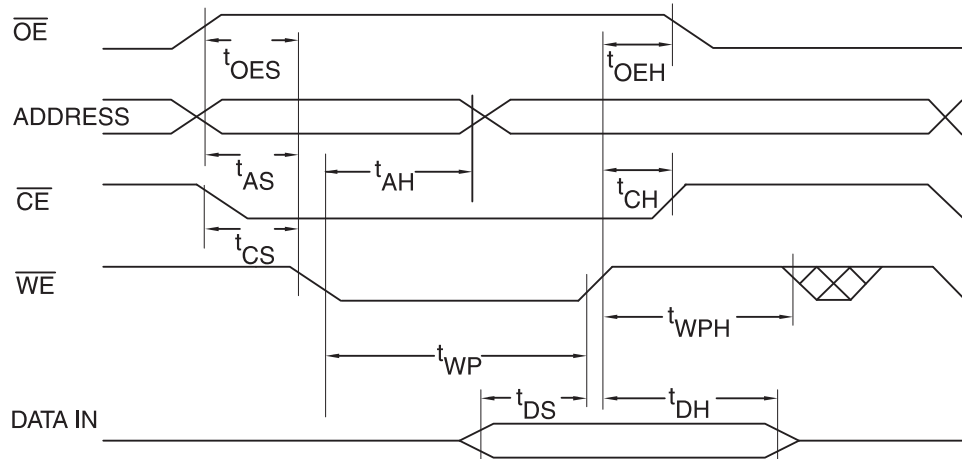
Note: 1. This parameter is characterized and is not 100% tested

AC Word Load Characteristics

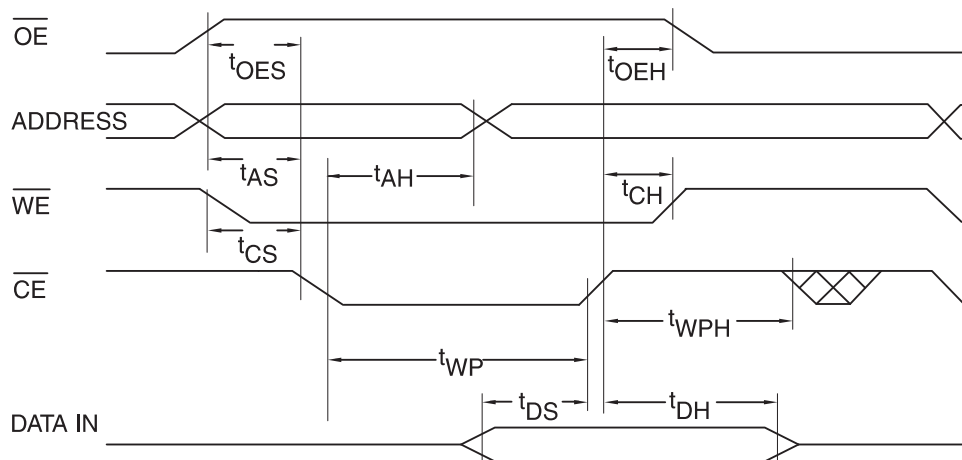
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, \overline{OE} Setup Time	0		ns
t_{AH}	Address Hold Time	40		ns
t_{CS}	Chip Select Setup Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width (\overline{WE} or \overline{CE})	40		ns
t_{DS}	Data Setup Time	30		ns
t_{DH}, t_{OEH}	Data, \overline{OE} Hold Time	0		ns
t_{WPH}	Write Pulse Width High	30		ns

AC Word Load Waveforms

\overline{WE} Controlled



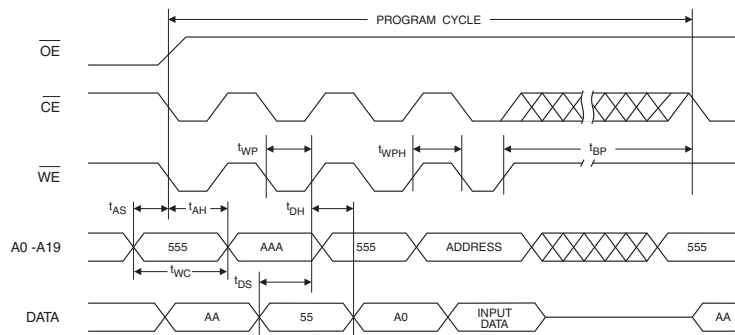
\overline{CE} Controlled



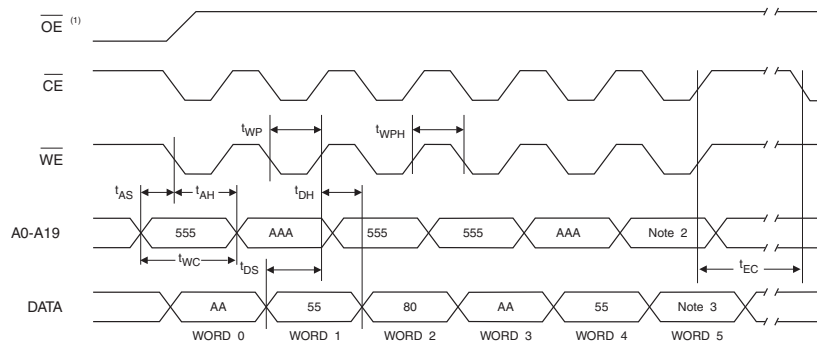
Program Cycle Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{BP}	Word Programming Time ($V_{IHPP} < V_{PP} < 4.5V$)		20	200	μs
t_{BPVPP}	Word Programming Time ($V_{PP} \geq 4.5V$)		10	100	μs
t_{AS}	Address Setup Time	0			ns
t_{AH}	Address Hold Time	40			ns
t_{DS}	Data Setup Time	30			ns
t_{DH}	Data Hold Time	0			ns
t_{WP}	Write Pulse Width	40			ns
t_{WPH}	Write Pulse Width High	30			ns
t_{WC}	Write Cycle Time	70			ns
t_{RP}	Reset Pulse Width	500			ns
t_{RH}	Reset High Time before Read	50			ns
t_{EC}	Chip Erase Cycle Time ($V_{PP} < 4.5V$)			12	seconds
t_{ECVPP}	Chip Erase Cycle Time ($V_{PP} \geq 4.5V$)			6	seconds
t_{SEC}	Sector Erase Cycle Time		300	400	ms

Program Cycle Waveforms



Sector or Chip Erase Cycle Waveforms



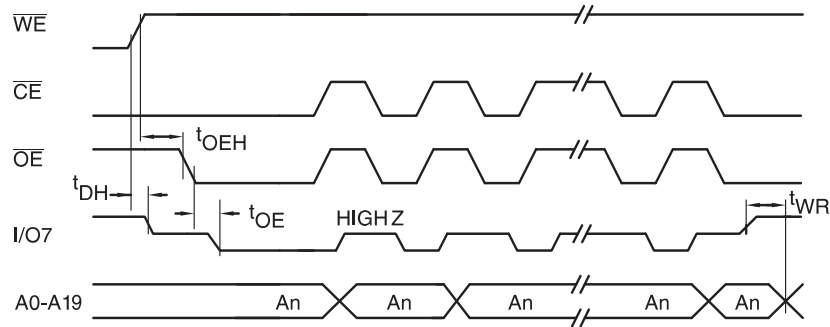
- Notes:
- \overline{OE} must be high only when \overline{WE} and \overline{CE} are both low.
 - For chip erase, the address should be 555. For sector erase, the address depends on what sector is to be erased. (See note 3 under Command Definitions.)
 - For chip erase, the data should be 10H, and for sector erase, the data should be 30H.

Data Polling Characteristics⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
$t_{OE\bar{H}}$	$\bar{O}\bar{E}$ Hold Time	10			ns
t_{OE}	$\bar{O}\bar{E}$ to Output Delay ⁽²⁾				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in "AC Read Characteristics" on page 14.

Data Polling Waveforms

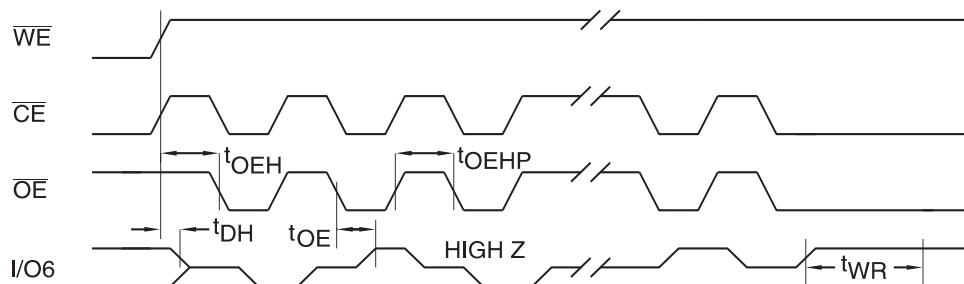


Toggle Bit Characteristics⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
$t_{OE\bar{H}}$	$\bar{O}\bar{E}$ Hold Time	10			ns
t_{OE}	$\bar{O}\bar{E}$ to Output Delay ⁽²⁾				ns
t_{OEHP}	$\bar{O}\bar{E}$ High Pulse	50			ns
t_{WR}	Write Recovery Time	0			ns

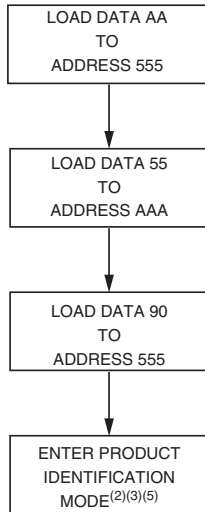
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in "AC Read Characteristics" on page 14.

Toggle Bit Waveforms⁽¹⁾⁽²⁾⁽³⁾

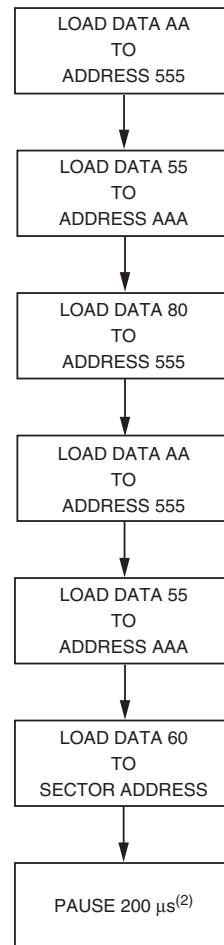


Notes: 1. Toggling either $\bar{O}\bar{E}$ or $\bar{C}\bar{E}$ or both $\bar{O}\bar{E}$ and $\bar{C}\bar{E}$ will operate toggle bit.
The t_{OEHP} specification must be met by the toggling input(s).
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

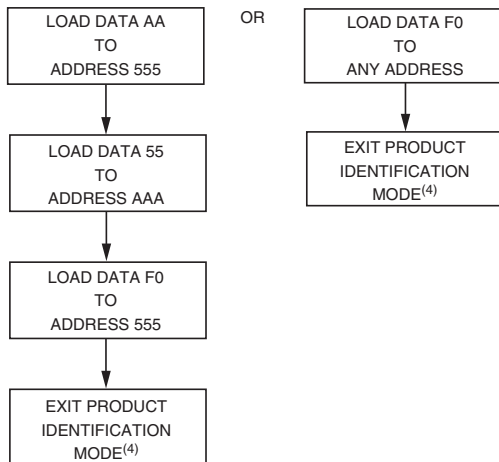
Software Product Identification Entry⁽¹⁾



Sector Lockdown Enable Algorithm⁽¹⁾



Software Product Identification Exit⁽¹⁾⁽⁶⁾



- Notes: 1. Data Format: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex)
 Address Format: A11 - A0 (Hex), A-1, and A11 - A19 (Don't Care).
 2. Sector Lockdown feature enabled.

- Notes: 1. Data Format: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex)
 Address Format: A11 - A0 (Hex), A-1, and A11 - A19 (Don't Care).
 2. A1 - A19 = V_{IL}. Manufacturer Code is read for A0 = V_{IL}; Device Code is read for A0 = V_{IH}. Additional Device Code is read for address 0003H
 3. The device does not remain in identification mode if powered down.
 4. The device returns to standard operation mode.
 5. Manufacturer Code: 1FH(x8); 001FH(x16)
 Device Code: C2H (x8); 00C2H (x16).
 Additional Device Code: 08H (x8); 0008H (x16)
 6. Either one of the Product ID Exit commands can be used.



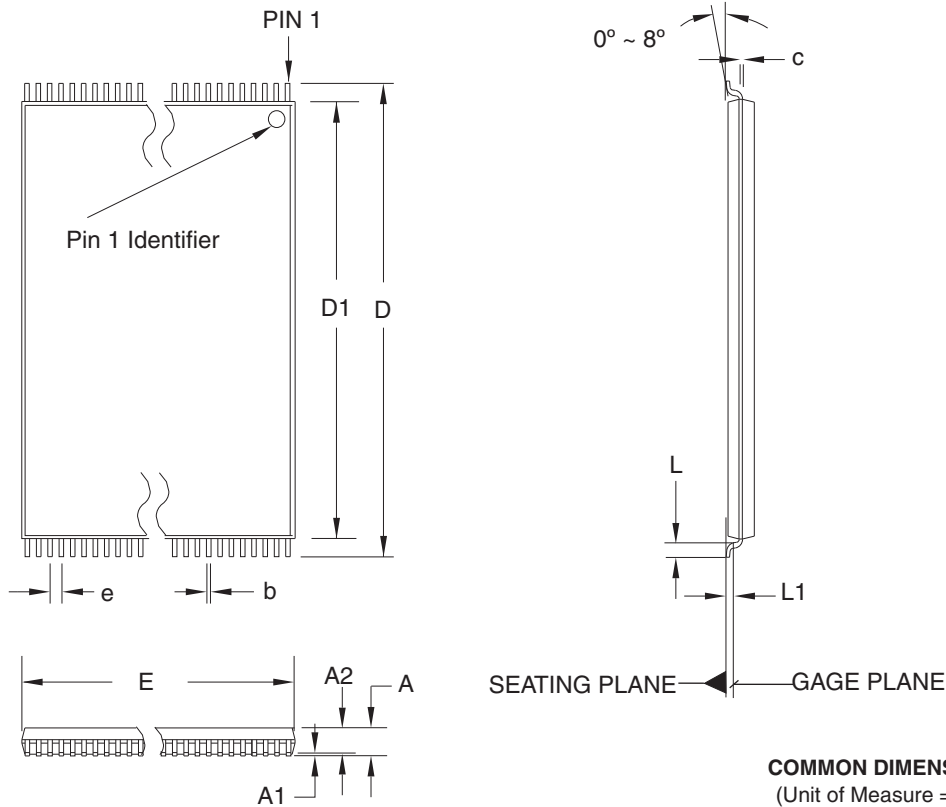
Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	25	0.01	AT47BV161T-70TI	48T	Industrial (-40° to 85° C)
90	25	0.01	AT47BV161T-90TI	48T	Industrial (-40° to 85° C)

Package Type	
48T	48-lead, Plastic Thin Small Outline Package (TSOP)

Packaging Information

48T – TSOP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	19.80	20.00	20.20	
D1	18.30	18.40	18.50	Note 2
E	11.90	12.00	12.10	Note 2
L	0.50	0.60	0.70	
L1	0.25 BASIC			
b	0.17	0.22	0.27	
c	0.10	–	0.21	
e	0.50 BASIC			

- Notes:
1. This package conforms to JEDEC reference MO-142, Variation DD.
 2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
 3. Lead coplanarity is 0.10 mm maximum.

10/18/01



2325 Orchard Parkway
San Jose, CA 95131

TITLE

48T, 48-lead (12 x 20 mm Package) Plastic Thin Small Outline Package, Type I (TSOP)

DRAWING NO.

48T

REV.

B





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